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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,900	08/20/2003	David Vinke	03-0862 81575	8193

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EXAMINER
GANDHI, DIPAKKUMAR B

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,900	VINKE ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicants' request for reconsideration filed on 2/27/2006 has been reviewed.

2. Amendment filed on 2/27/2006 has been entered.

3. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 2, 7, 8, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Si et al. (US 4,819,166) in view of Cliff et al. (US 6,023,439) and Tomita (US 6,442,092 B1).

As per claim 1, Si et al. teach a latch based random access memory comprising a latch array (fig. 2, 6, col. 3, lines 6-11, col. 9, lines 26-29, Si et al.).

However Si et al. do not explicitly teach the specific use of an input data register; an input data buffer coupled to the input data register; an array coupled to the input data buffer.

Cliff et al. in an analogous art teach that RAM block 447 interfaces block 448 (fig. 21B, col. 16, line 15, Cliff et al.). Cliff et al. also teach that the user data...top interface 448 (fig. 21A, col. 16, lines 45-50, Cliff et al.). Cliff et al. teach that the one memory block...memory array (col. 26, lines 7-14, Cliff et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Si et al.'s patent with the teachings of Cliff et al. by including an additional step of using an input data register; an input data buffer coupled to the input data register; an array coupled to the input data buffer.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using an input data register; an input data buffer coupled to the input data register; an array coupled to the input data buffer would provide the opportunity to store the input data in a temporary storage location before it is written in the memory array.

Si et al. also do not explicitly teach the specific use of a latch array bypass multiplexer for selecting one of the input data buffer and the latch array to generate a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal.

However Tomita in an analogous art teaches that referring to FIG. 6, the TAP circuit...TAP controller 74 (col. 8, lines 15-20, Tomita). Tomita also teaches that the multiplexer 70...the TDO terminal (col. 8, lines 45-52, Tomita).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Si et al.'s patent with the teachings of Tomita by including an additional step of using a latch array bypass multiplexer for selecting one of the input data buffer and the latch array to generate a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to selectively conduct logic scan testing and memory scan testing.

- As per claim 2, Si et al., Cliff et al. and Tomita teach the additional limitations.

Tomita teaches a read address register; and a read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal (fig. 6, 12, col. 8, lines 15-20, col. 10, lines 48-65, Tomita)

- As per claim 7, Si et al., Cliff et al. and Tomita teach the additional limitations.

Si et al. teach a latch based random access memory in an integrated circuit die (fig. 2, 6, col. 3, lines 6-11, col. 9, lines 26-29, Si et al.).

Cliff et al. teach an input data buffer of the random access memory (fig. 21A, 21B, col. 16, line 15, lines 45-50, col. 26, lines 7-14, Cliff et al.).

Tomita teaches a method of scan testing comprising steps of: (a) modifying a memory to include an array bypass multiplexer for selecting one of data buffer of the random access memory and an array of the random access memory for generating a first data output of the random access memory from the input data buffer during logic scan testing and a second data output of the random access memory from the array during memory scan testing in response to a memory scan mode signal; (b) asserting the memory scan mode signal during a memory scan test; and (c) removing the memory scan mode signal during a logic scan test (fig. 6, 12, col. 8, lines 15-20, col. 10, line 48 to col. 11, line 14, Tomita).

- As per claim 8, Si et al., Cliff et al. and Tomita teach the additional limitations.

Tomita teaches a step of selecting one of a logic scan address and a memory scan address for coupling to a read address register of the latch based random access memory in response to the memory scan mode signal (col. 10, lines 48-65, Tomita).

- As per claim 12, Si et al., Cliff et al. and Tomita teach the additional limitations.

Tomita teaches bypassing logic chains surrounding the latch based random access memory during a memory scan test (fig. 6, col. 8, lines 45-52, col. 10, line 66 to col. 11, line 14, Tomita).

- As per claim 13, Si et al., Cliff et al. and Tomita teach the additional limitations.

Tomita teaches bypassing the latch array during a logic scan test (col. 8, lines 14-19, lines 45-52, Tomita).

7. Claims 3, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Si et al. (US 4,819,166), Cliff et al. (US 6,023,439) and Tomita (US 6,442,092 B1) as applied to claim 2 above, and further in view of Lach et al. (US 5,909,451).

As per claim 3, Si et al., Cliff et al. and Tomita substantially teach the claimed invention described in claim 2 (as rejected above). Si et al. teach a write enable register and the read address register (fig. 2, 5, col. 3, lines 28-33, col. 5, lines 55-58, Si et al.).

However Si et al., Cliff et al. and Tomita do not explicitly teach the specific use of a clock signal multiplexer coupled to for selecting one of a scan test clock signal and an application specific clock signal in response to a scan mode signal.

Lach et al. in an analogous art teach that SCAN IN/OUT MODE signal...during those operations (fig. 3, col. 13, lines 1-21, Lach et al.). Lach et al. also teach that the clock signal multiplexers 55(d) and 56(e)...the scan chain (col. 13, lines 46-52, Lach et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Si et al.'s patent with the teachings of Lach et al. by including an additional step of using a clock signal multiplexer coupled to for selecting one of a scan test clock signal and an application specific clock signal in response to a scan mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to select read/write clock signal or scan test clock signal depending on scan mode.

- As per claim 9, Si et al., Cliff et al., Tomita and Lach et al. teach the additional limitations.

Lach et al. teach a step of selecting one of a scan test clock signal and an application-specific clock signal in response to a scan mode signal (fig. 3, col. 13, lines 1-21, col. 13, lines 46-52, Lach et al.).

Si et al. teach a write address register and the read address register of the latch based random access memory (fig. 2, 5, col. 3, lines 28-33, col. 5, lines 55-59, Si et al.).

8. Claims 4, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Si et al. (US 4,819,166), Cliff et al. (US 6,023,439), Tomita (US 6,442,092 B1) and Lach et al. (US 5,909,451) as applied to claim 3 above, and further in view of Sindhu (US 5,123,101).

As per claim 4, Si et al., Cliff et al., Tomita and Lach et al. substantially teach the claimed invention described in claim 3 (as rejected above).

However Si et al., Cliff et al., Tomita and Lach et al. do not explicitly teach the specific use of bypass logic for controlling the latch array bypass multiplexer.

Sindhu in an analogous art teaches that bypass logic 136 generates an RP and flags for bypass multiplexer 138 (fig. 4, col. 12, lines 34-35, Sindhu). Sindhu also teaches that the bypass register...bypass multiplexer 138 (fig. 4, col. 16, lines 47-51, Sindhu).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Si et al.'s patent with the teachings of Sindhu by including an additional step of using bypass logic for controlling the latch array bypass multiplexer.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using bypass logic for controlling the latch array bypass multiplexer would provide the opportunity to apply external control signals to the latch array bypass multiplexer.

- As per claim 10, Si et al., Cliff et al., Tomita, Lach et al. and Sindhu teach the additional limitations.

Sindhu teaches a step of controlling bypass multiplexer (fig. 4, col. 12, lines 34-35, col. 16, lines 47-51, Sindhu).

Si et al. teaches the latch array (fig. 2, 6, col. 3, lines 6-11, col. 9, lines 26-29, Si et al.).

9. Claims 5, 6, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Si et al. (US 4,819,166), Cliff et al. (US 6,023,439), Tomita (US 6,442,092 B1) and Lach et al. (US 5,909,451) as applied to claim 3 above, and further in view of Lindkvist (US 6,698,005 B2).

As per claim 5, Si et al., Cliff et al., Tomita and Lach et al. substantially teach the claimed invention described in claim 3 (as rejected above).

However Si et al., Cliff et al., Tomita and Lach et al. do not explicitly teach the specific use of a lockup latch coupled to the read address register for providing a minimum hold time for the write enable register during scan testing of the latch based random access memory.

Lindkvist in an analogous art teaches that timing change...destination register 111 (fig. 5, col. 5, lines 37-43, Lindkvist).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Si et al.'s patent with the teachings of Lindkvist by including an additional step of using a lockup latch coupled to the read address register for providing a minimum hold time for the write enable register during scan testing of the latch based random access memory.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to resolve the timing problem and delay an input to a register.

- As per claim 6, Si et al., Cliff et al., Tomita, Lach et al. and Lindkvist teach the additional limitations.

Lindkvist teaches a lockup latch coupled to the input data register for providing a minimum hold time during scan testing of the latch based random access memory (fig. 5, col. 5, lines 37-43, Lindkvist).

- As per claim 11, Si et al., Cliff et al., Tomita, Lach et al. and Lindkvist teach the additional limitations.

Lindkvist teaches a step of providing a minimum hold time (fig. 5, col. 5, lines 37-43, Lindkvist).

Si et al. teach the latch based random access memory (fig. 2, 6, col. 3, lines 6-11, col. 9, lines 26-29, Si et al.).

Tomita teaches scan testing of the random access memory (abstract, Tomita).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

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PRIMARY EXAMINER